IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

"EXPRESS MAIL" MAILING LABEL NUMBER EL 768537349 US

In re Patent Application of:
ROCHE ET AL.

Serial No. **Not yet assigned**

Filing Date: **Herewith**

For: **SYNCHRONOUS DATA TRANSMISSION METHOD**

DATE OF DEPOSIT Nov. 7, 2001

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PRELIMINARY AMENDMENT

Director, U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Prior to the calculation of fees and examination of the present application, please enter the amendments and remarks set out below.

In the Drawings:

Submitted herewith is a request for a proposed drawing modification as indicated in red ink to correct minor informalities in FIGs. 2A, 2B, 4A and 4B.

In the Claims:

Please cancel Claims 1 to 19.

Please add new Claims 20 to 52.

20. A method of transmitting data between two devices via a clock line and at least one data line, the clock line being maintained by default on a first logic value, the method comprising:

providing each device with the ability to tie the clock line to a potential representing a second logic value opposite the first logic value;

tying the clock line to the second logic value, via the two devices, when data is transmitted;

maintaining the tie to the clock line by the device to which the data is sent while the device has not read the data; and

maintaining the data on the data line by the device sending the data at least until an instant when the clock line is released by the device to which the data is sent.

21. A method according to Claim 20, wherein one of the two devices is a master device and the other is a slave device, the master device tying the clock line to the second logic value before the slave device when data is transmitted, regardless of the direction in which the data is transmitted.

22. A method according to Claim 21, wherein the master device ties the clock line to the second logic value after applying data to the data line when the master device is sending the data to the slave device.

23. A method according to Claim 22, wherein the slave device detects the second logic value on the clock line,

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then ties the clock line to the second logic value and reads the data, when the slave device is receiving the data from the master device.

24. A method according to Claim 23, wherein a time period that the slave device has to release the clock line after receiving data, is independent of any action by the master device, as the master device does not send any new data while the slave device has not released the clock line.

25. A method according to Claim 21, wherein the master device ties the clock line to the second logic value when the master receives data from the slave device.

26. A method according to Claim 25, wherein the slave device detects the second logic value on the clock line, then ties the clock line to the second logic value, and applies the data to the data line, when the slave device is sending data to the master device.

27. A method according to Claim 26, wherein a time period that the slave device has to release the clock line after sending the data, is independent of any action by the master device, as the master device does not tie the clock line to the second logic value to request a new data until the slave device has released the clock line.

28. A method according to Claim 21, wherein when the clock line has the first logic value, a time period that

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the master device has to tie the clock line to the second logic value is independent of any action by the slave device.

29. A method according to Claim 21, further comprising providing the slave device with a communication interface circuit including:

trigger means for automatically tying the clock line to the second logic value when the clock line is changing from the first logic value to the second logic value;

an input for applying a clock line release signal to the trigger means; and

an output for delivering a status signal that has a first value when the clock line is tied to the second logic value by the trigger means and a second value when the clock line is released by the trigger means.

30. A method according to Claim 29, wherein the communication interface circuit further comprises:

means for storing at least one data; and

means for automatically applying the at least one stored data to the data line when the clock line changes from the first logic value to the second logic value.

31. A method according to Claim 20, wherein the first logic value is 1 and the second logic value is 0.

32. A method of transmitting data between two devices connected via a clock line and at least one data line, the method comprising:

maintaining the clock line on a first logic value as a default;

providing each device with the ability to tie the clock line to a potential representing a second logic value;

tying the clock line to the second logic value, via the two devices, when data is transmitted;

maintaining the tie to the clock line by the device to which the data is sent while the device has not read the data; and

maintaining the data on the data line by the device sending the data at least until the clock line is released by the device to which the data is sent.

33. A method according to Claim 32, wherein one of the two devices is a master device and the other is a slave device, the master device tying the clock line to the second logic value before the slave device when data is transmitted, regardless of the direction in which the data is transmitted.

34. A method according to Claim 33, wherein the master device ties the clock line to the second logic value after applying data to the data line when the master device is sending the data to the slave device.

35. A method according to Claim 34, wherein the slave device detects the second logic value on the clock line, then ties the clock line to the second logic value and reads the data, when the slave device is receiving the data from the master device.

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36. A method according to Claim 35, wherein a time period that the slave device has to release the clock line after receiving data, is independent of any action by the master device, as the master device does not send any new data while the slave device has not released the clock line.

37. A method according to Claim 33, wherein the master device ties the clock line to the second logic value when the master receives data from the slave device.

38. A method according to Claim 37, wherein the slave device detects the second logic value on the clock line, then ties the clock line to the second logic value, and applies the data to the data line, when the slave device is sending data to the master device.

39. A method according to Claim 38, wherein a time period that the slave device has to release the clock line after sending the data, is independent of any action by the master device, as the master device does not tie the clock line to the second logic value to request a new data until the slave device has released the clock line.

40. A method according to Claim 33, wherein when the clock line has the first logic value, a time period that the master device has to tie the clock line to the second logic value is independent of any action by the slave device.

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41. A method according to Claim 33, further comprising providing the slave device with a communication interface circuit including:

a trigger circuit for automatically tying the clock line to the second logic value when the clock line is changing from the first logic value to the second logic value;

an input for applying a clock line release signal to the trigger circuit; and

an output for delivering a status signal that has a first value when the clock line is tied to the second logic value by the trigger circuit and a second value when the clock line is released by the trigger circuit.

42. A method according to Claim 41, wherein the communication interface circuit further comprises:

a buffer for storing at least one data; and

a circuit for automatically applying the at least one stored data to the data line when the clock line changes from the first logic value to the second logic value.

43. A method according to Claim 32, wherein the first logic value is 1 and the second logic value is 0.

44. A data transmitting/receiving device comprising:

a clock line connection terminal for connection to a clock line;

at least one data line connection terminal for connection to a data line;

means for tying the clock line to a potential representing a second logic value that is the opposite of a first logic value; and

data sending means for waiting for the clock line to have the first logic value, applying data to the data line, tying the clock line to the second logic value, then releasing the clock line, and maintaining the data on the data line at least until the clock line has the first logic value, when the data is to be sent.

45. A device according to Claim 44, further comprising data receiving means for waiting for the clock line to have the first logic value, tying the clock line to the second logic value, reading data on the data line, then releasing the clock line, when the data is to be received.

46. A data transmitting/receiving device comprising:

a clock line connection terminal for connection to a clock line;

at least one data line connection terminal for connection to a data line;

means for tying the clock line to a potential representing a second logic value that is the opposite of a first logic value; and

means for detecting a change from the first logic value to the second logic value on the clock line, tying the clock line to the second logic value, reading data on the data

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line, and releasing the clock line, when the data is to be received.

47. A device according to Claim 46, further comprising means for detecting a change from the first logic value to the second logic value on the clock line, tying the clock line the second logic value, applying data to the data line, and releasing the clock line, when the data is to be sent.

48. A synchronous data transmission system comprising:

a clock line;

a data line;

a master data transmitting/receiving device comprising

a clock line connection terminal connected to the clock line,

at least one data line connection terminal connected to the data line,

means for tying the clock line to a potential representing a second logic value that is the opposite of a first logic value, and

data sending means for waiting for the clock line to have the first logic value, applying data to the data line, tying the clock line to the second logic value, then releasing the clock line, and maintaining the data on the data line at least until

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the clock line has the first logic value, when the data is to be sent; and

a slave data transmitting/receiving device comprising

a clock line connection terminal connected to the clock line;

at least one data line connection terminal connected to the data line;

means for tying the clock line to the potential representing the second logic value; and

means for detecting a change from the first logic value to the second logic value on the clock line, tying the clock line to the second logic value, reading the data on the data line, and releasing the clock line, when the data is to be received.

49. A system according to Claim 48, wherein the master device further comprises data receiving means for waiting for the clock line to have the first logic value, tying the clock line to the second logic value, reading the data on the data line, then releasing the clock line, when the data is to be received by the master device.

50. A system according to Claim 48, wherein the slave device further comprises means for detecting a change from the first logic value to the second logic value on the clock line, tying the clock line the second logic value,

applying the data to the data line, and releasing the clock line, when the data is to be sent from the slave device.

51. A communication interface circuit for connection to a data transmitting/receiving device via a clock line and at least one data line, the circuit comprising:

means for tying the clock line to a potential representing a second logic value that is the opposite of a first logic value;

trigger means for automatically tying the clock line to the second logic value when the clock line is changing from the first logic value to the second logic value;

an input to apply a clock line release signal to the trigger means; and

an output to deliver an information signal that has a first value when the clock line is tied to the second logic signal by the trigger means and a second value when the clock line is released by the trigger means.

52. A communication interface circuit according to Claim 51 further comprising:

means for storing data; and

means for automatically applying the data to the data line when the clock line changes from the first logic value to the second logic value.

REMARKS

It is believed that all of the claims are patentable over the prior art. For better readability and the Examiner's

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convenience, the newly submitted claims differ from the translated counterpart claims which are being canceled. The newly submitted claims do not represent changes or amendments that narrow the claim scope for any reason related to the statutory requirements for patentability.

Accordingly, after the Examiner completes a thorough examination, a Notice of Allowance is respectfully requested in due course. If any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number below.

Respectfully submitted,

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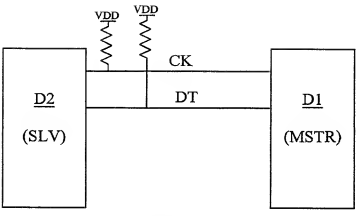

FIG. 1

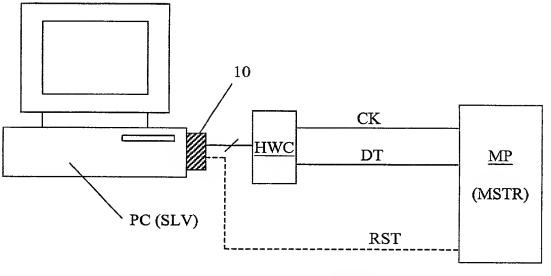

FIG. 7

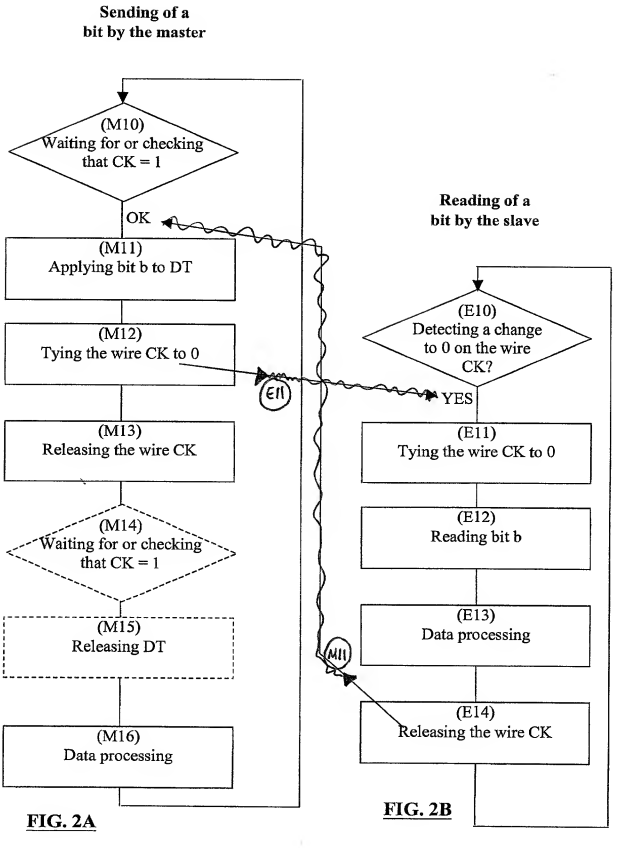
Sending of a bit by the master
(M10) Waiting for or checking that CK = 1
OK
(M11) Applying bit b to DT
(M12) Tying the wire CK to 0
(M13) Releasing the wire CK
(M14) Waiting for or checking that CK = 1
(M15) Releasing DT
(M16) Data processing
Reading of a bit by the slave
(E10) Detecting a change to 0 on the wire CK?
YES
(E11) Tying the wire CK to 0
(E12) Reading bit b
(E13) Data processing
(E14) Releasing the wire CK

FIG. 2A

FIG. 2B

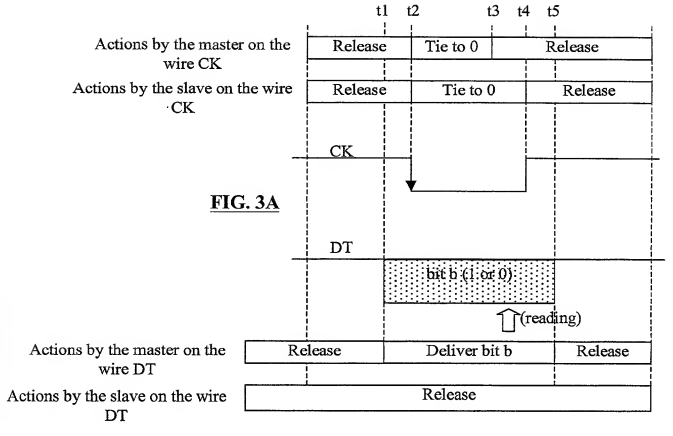
t1
t2
t3
t4
t5
Actions by the master on the wire CK
Release
Tie to 0
Release
Actions by the slave on the wire CK
Release
Tie to 0
Release
CK
DT
bit b (1 or 0)
(reading)
Actions by the master on the wire DT
Release
Deliver bit b
Release
Actions by the slave on the wire DT
Release

FIG. 3A

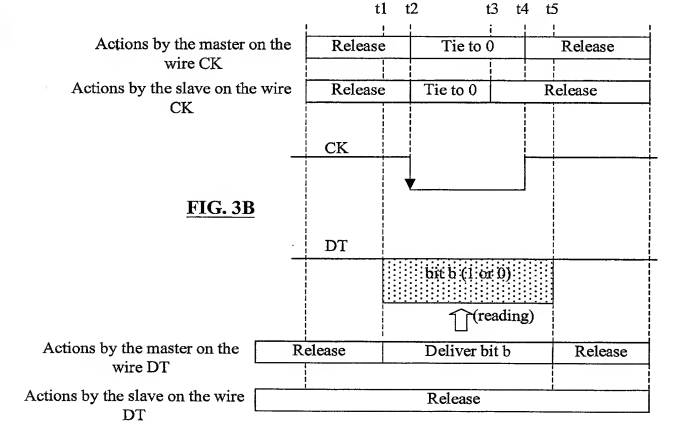
t1
t2
t3
t4
t5
Actions by the master on the wire CK
Release
Tie to 0
Release
Actions by the slave on the wire CK
Release
Tie to 0
Release
CK
DT
bit b (1 or 0)
(reading)
Actions by the master on the wire DT
Release
Deliver bit b
Release
Actions by the slave on the wire DT
Release

FIG. 3B

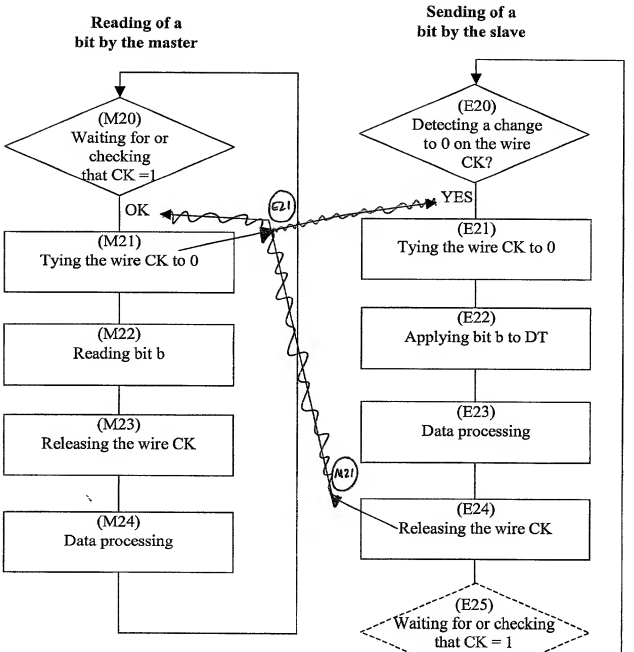
Reading of a bit by the master
Sending of a bit by the slave
(M20) Waiting for or checking that CK =1
OK
(M21) Tying the wire CK to 0
(M22) Reading bit b
(M23) Releasing the wire CK
(M24) Data processing
(E20) Detecting a change to 0 on the wire CK?
YES
(E21) Tying the wire CK to 0
(E22) Applying bit b to DT
(E23) Data processing
(E24) Releasing the wire CK
(E25) Waiting for or checking that CK = 1
(E26) Releasing DT
G21
N21

FIG. 4A

FIG. 4B

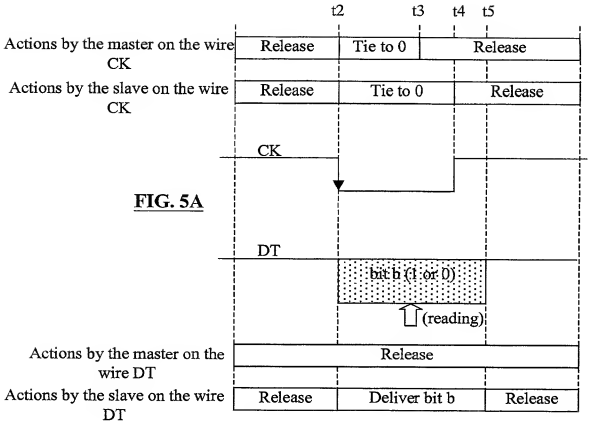
t2
t3
t4
t5
Actions by the master on the wire CK
Release
Tie to 0
Release
Actions by the slave on the wire CK
Release
Tie to 0
Release
CK
DT
bit b (1 or 0)
(reading)
Actions by the master on the wire DT
Release
Actions by the slave on the wire DT
Release
Deliver bit b
Release

FIG. 5A

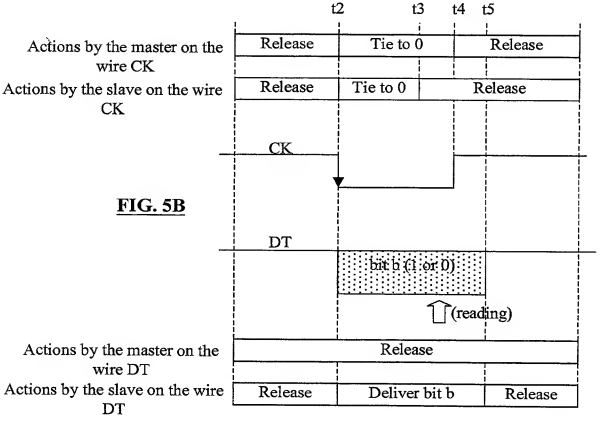
t2
t3
t4
t5
Actions by the master on the wire CK
Release
Tie to 0
Release
Actions by the slave on the wire CK
Release
Tie to 0
Release
CK
DT
bit b (1 or 0)
(reading)
Actions by the master on the wire DT
Release
Actions by the slave on the wire DT
Release
Deliver bit b
Release

FIG. 5B

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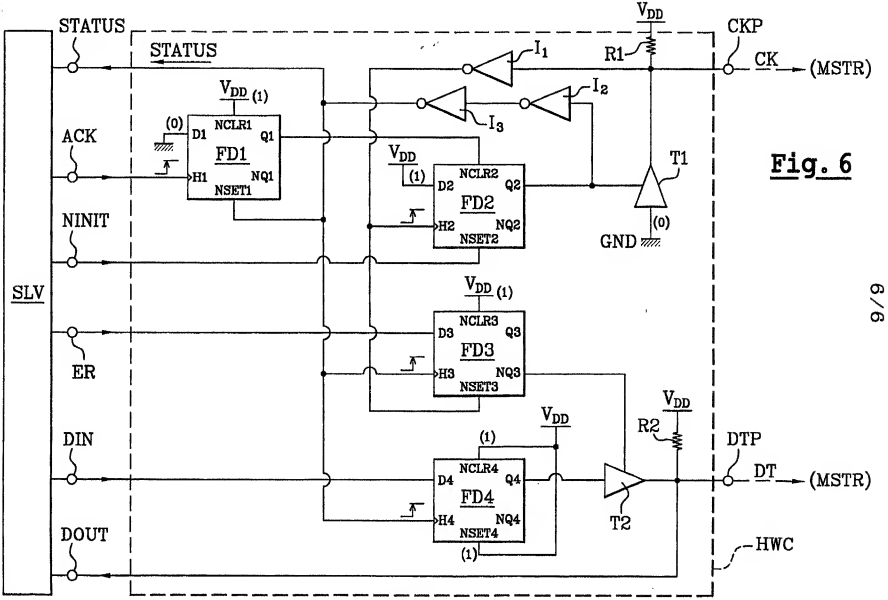

Fig. 6